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HIGH PERFORMANCE MAC BASED ON MULTI-LEVEL APPROXIMATE COMPRESSORS WITH BALANCED ERROR ACCUMULATION

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ABSTRACT

It is presented a unique approximate computing approach for implementing energy-efficient multiply-accumulate (MAC) processing. We use different approximate multipliers in an interleaved manner to mitigate mistakes in the opposite direction during accumulate operations, in contrast to previous efforts that suffer from error accumulation restricting the approximation range. We first build approximation 4-2 compressors that generate error in the opposite direction while minimizing computing costs for balanced error accumulation. Positive and negative multipliers are then carefully built based on the probabilistic analysis to produce a similar error distance. Further, additional to 4-2 compressors 5-2, 6-3 and 7-3 approximate compressors and counters are also used to optimize area and power. Simulation findings on a variety of real-world applications show that the proposed MAC processing extends the range of approximate components, resulting in a more energy-efficient computing situation. Even when compared to state-of-the-art alternatives, the suggested interleaving scheme reduces the latest CNN accelerator's core-level energy consumption by more than 35% without compromising recognition accuracy.

KEYWORDS: *Approximate Computing, Convolutional Neural Network, Image Processing, Low-Power Circuit Design, Multiplier*